



GENERAL DESCRIPTION

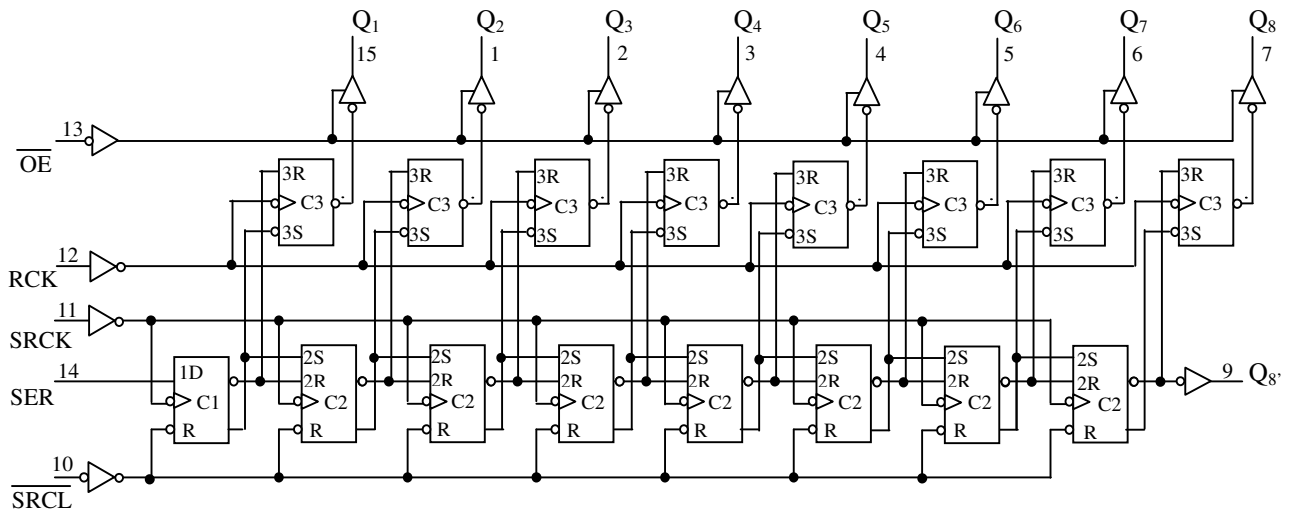
HC595 is fabricated with high-speed silicon gate CMOS technology. It contains an 8-bit serial-in, serial or parallel-out shift register and an 8-bit D-type storage register with parallel 3-state outputs. The shift and storage register have independent clock inputs. Both the shift register clock (SRCK) and storage register clock (RCK) are positive-edge triggered.

The shift register has a direct overriding clear input (SRCL), serial data input (SER), and serial outputs for cascading. When the output-enable (OE) input is high, the outputs are in the high-impedance state. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

FEATURES

- 8-bit serial-in, parallel-out shift register with storage
- Shift register has direct clear
- 8-bit D-type storage register with parallel 3-state outputs
- Two independent clocks for shift and storage register
- Wide operating power supply voltage 2-6V
- Low input current < 1µA
- Low power consumption, Max. 80µA (74HC595)
- Output driving capacity ± 6 mA at 5V
- Typical propagation delay 13nS

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

1. Truth Table

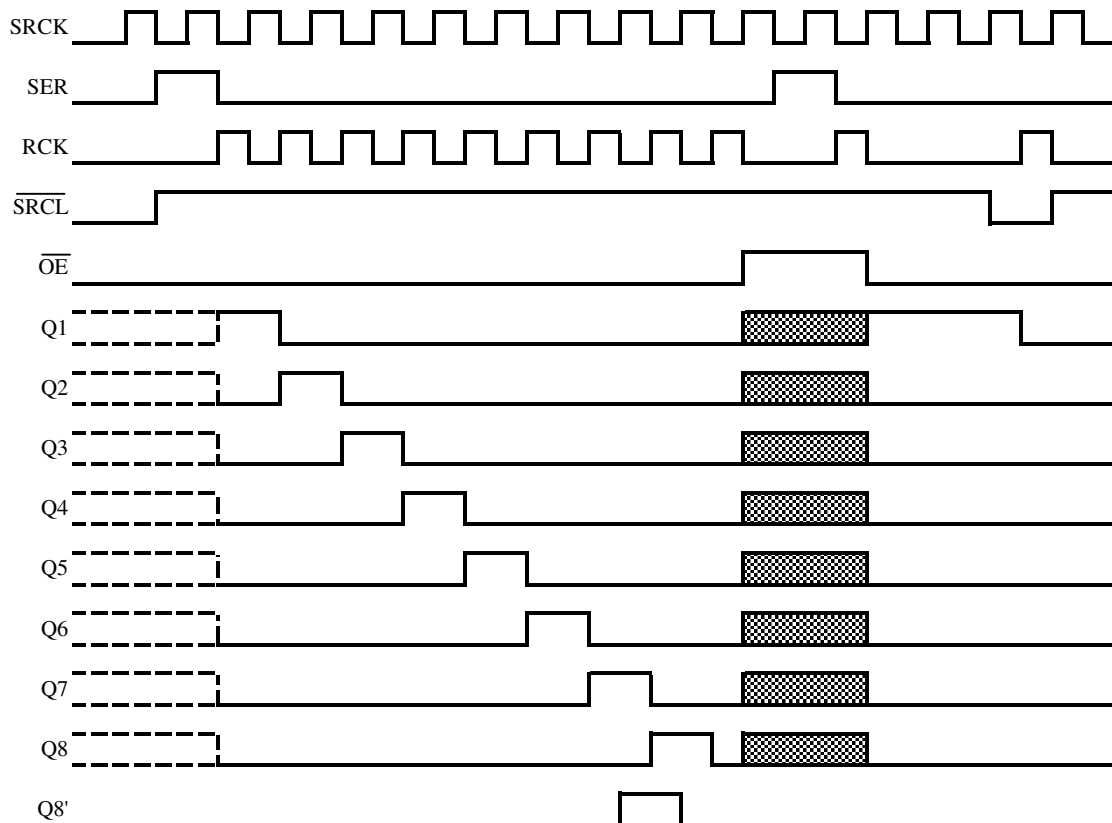
Inputs					Function
SER	SRCK	$\overline{\text{SRCL}}$	RCK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q1-Q8 are disabled.
X	X	X	X	L	Outputs Q1-Q8 are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the latch.


H = High Level (steady state). L= Low Level (steady state)

X = Irrelevant (don't care)

↑ = Transition from low to high level.

2. Logic Waveform



Note:  implies that the outputs are in 3-state mode.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Value	Unit
DC supply voltage Vcc	- 0.5 ~ + 7.0	V
DC input clamp current I <sub>ik</sub> (V <sub>i</sub> <0 or V <sub>i</sub> >V <sub>cc</sub> )	±20	mA
DC output clamp current I <sub>ok</sub> (V <sub>o</sub> <0 or V <sub>o</sub> >V <sub>cc</sub> )	±20	mA
DC Current Drain per pin, any output (I <sub>out</sub> )	±35	mA
DC supply Current, Vcc or GND (I <sub>cc</sub> )	±70	mA
Storage Temperature( T <sub>stg</sub> )	-65 ~ +150	°C
Lead Temperature(T <sub>L</sub> ) (Soldering, 10seconds)	260	°C

**Note:**

1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

**RECOMMENDED OPERATING CONDITONS**

Parameter		Min.	Normal	Max.	Unit
Power Supply Voltage (Vcc)		2	5	6	V
V <sub>IH</sub> High-level input voltage	VCC=2.0V	1.5			V
	VCC=4.5V	3.15			
	VCC=6.0V	4.2			
V <sub>IL</sub> Low-level Input Voltage	VCC=2.0V			0.5	V
	VCC=4.5V			1.35	
	VCC=6.0V			1.8	
V <sub>I</sub> Input Voltage		0		V <sub>cc</sub>	V
V <sub>o</sub> Output Voltage		0		V <sub>cc</sub>	V
Operating Temperature (TA)	74HC595	-40		85	°C
	54HC595	-55		125	°C
Input Rise/Fall Times (tr, tf)	VCC=2.0V			1000	ns
	VCC=4.5V			500	
	VCC=6.0V			400	

**Note:**

2. All unused inputs of the device must be held at V<sub>cc</sub> or GND to ensure proper device operation.
3. If this device is used in the threshold region (from V<sub>ILmax</sub> = 0.5 V to V<sub>IHmin</sub> = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>i</sub> = 1000 ns and V<sub>cc</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

**DC ELECTRICAL CHARACTERISTICS**

(Apply across temperature range unless otherwise specified)

PARAMETER	TEST CONDITIONS		V <sub>cc</sub>	TA = 25°C			54HC595		74HC595		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20uA	2 V	1.9	1.998		1.9		1.9	V		
			4.5V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		I <sub>OH</sub> = -6 mA	4.5V	3.98	4.3		3.7		3.84			
			6 V	5.48	5.8		5.2		5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20uA	2 V		0.002	0.1		0.1		V		
			4.5V		0.001	0.1		0.1			0.1	
			6 V		0.001	0.1		0.1			0.1	
		I <sub>OL</sub> = 6mA	4.5V		0.17	0.26		0.4			0.33	
			6 V		0.15	0.26		0.4			0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>cc</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA	
I <sub>oz</sub>	V <sub>O</sub> = V <sub>cc</sub> or 0, Q1-Q8		6 V		±0.01	±0.5		±10		±5	uA	
I <sub>cc</sub>	V <sub>I</sub> = V <sub>cc</sub> or 0 I <sub>O</sub> = 0		6 V					8		160	80	uA
C <sub>i</sub>			2V ~ 6V			3		10		10	10	pF

**TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)**

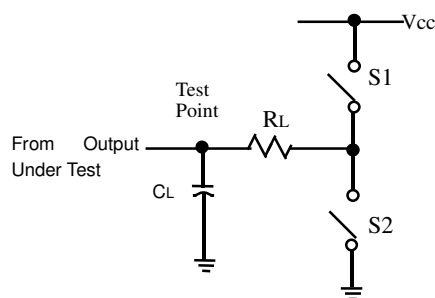
Parameter	Symbol	Unit	Guaranteed Limit			Test Condition
			TA=25°C	54HC595	74HC595	
Clock frequency	f <sub>clock</sub>	MHz	6	4.2	5	V <sub>cc</sub> =2.0V
			31	21	25	V <sub>cc</sub> =4.5V
			36	25	29	V <sub>cc</sub> =6.0V
Pulse duration	t <sub>w</sub>	ns	80	120	100	V <sub>cc</sub> =2.0V
			16	24	20	V <sub>cc</sub> =4.5V
			14	20	17	V <sub>cc</sub> =6.0V
			80	120	100	V <sub>cc</sub> =2.0V
			16	24	20	V <sub>cc</sub> =4.5V
			14	20	17	V <sub>cc</sub> =6.0V
Setup time	t <sub>su</sub>	ns	100	150	125	V <sub>cc</sub> =2.0V
			20	30	25	V <sub>cc</sub> =4.5V
			17	25	21	V <sub>cc</sub> =6.0V
			75	113	94	V <sub>cc</sub> =2.0V
			15	23	19	V <sub>cc</sub> =4.5V
			13	19	16	V <sub>cc</sub> =6.0V
			50	75	65	V <sub>cc</sub> =2.0V
			10	15	13	V <sub>cc</sub> =4.5V
			9	13	11	V <sub>cc</sub> =6.0V
			50	75	60	V <sub>cc</sub> =2.0V
10	15	12	V <sub>cc</sub> =4.5V			
9	13	11	V <sub>cc</sub> =6.0V			
Hold time,	t <sub>h</sub>	ns	0	0	0	V <sub>cc</sub> =2~6V

Note: . 4. This setup time allows the latch to receive stable data from the shift register. The clock can be connected together, in this case the shift register is one clock pulse ahead of the latch.

**AC ELECTRICAL CHARACTERISTICS (unless otherwise noted)**

Parameter	Symbol	From (Input)	To (Output)	Unit	Vcc	Ta = 25°C			54HC595		74HC595		Parameter					
						Min	Typ	Max	Min	Max	Min	Max						
Maximum clock frequency	fmax			MHz	2V	6	26		4.2		5	CL=50pF						
					4.5V	31	38		21		25							
					6V	36	42		25		29							
Maximum Propagation Delay (Clock to Q)	tpd	SRCK	Q8'	ns	2V		50	160		240		200	CL=50pF					
					4.5V		17	32		48		40						
					6V		14	27		41		34						
		LCK	Q1-Q8	ns	2V		50	150		225		187						
					4.5V		17	30		45		37						
					6V		14	26		38		32						
	LCK	Q1-Q8	ns	2V		60	200		300		250	CL=150pF						
				4.5V		22	40		60		50							
				6V		19	34		51		43							
Maximum Propagation Delay (SRCL to Q8')	tPHL	SRCL	QH'	ns	2V		51	175		261		219	CL=50pF					
					4.5V		18	35		52		44						
					6V		15	30		44		37						
Maximum Propagation Delay (OE to Q)	ten	OE	Q1-Q8	ns	2V		40	150		225		187	CL=50pF					
					4.5V		15	30		45		37						
					6V		13	26		38		32						
					tdis	OE	Q1-Q8	ns	2V		70	200			298		250	CL=150pF
									4.5V		23	40			60		50	
									6V		19	34			51		43	
	Maximum Output Rising and Falling Time	tt		Q1-Q8	ns	2V		28	60		90		75	CL=50pF				
						4.5V		8	12		18		15					
						6V		6	10		15		13					
Q8'				2V			28	75		110		95						
				4.5V			8	15		22		19						
				6V			6	13		19		16						
Q1-Q8		2V		45	210		315		265	CL=150pF								
		4.5V		17	42		63		53									
		6V		13	36		53		45									
Power Dissipation Capacitance	C <sub>PD</sub>			pF			400		-		-							

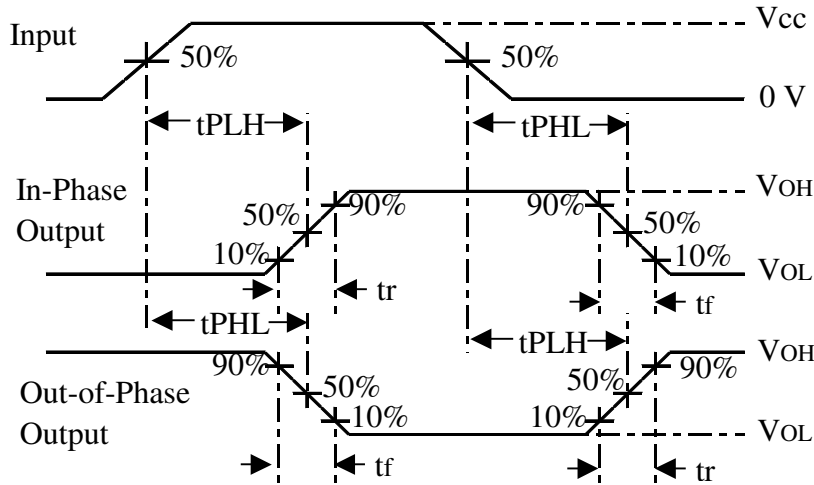
**PARAMETER MEASUREMENT INFORMATION**



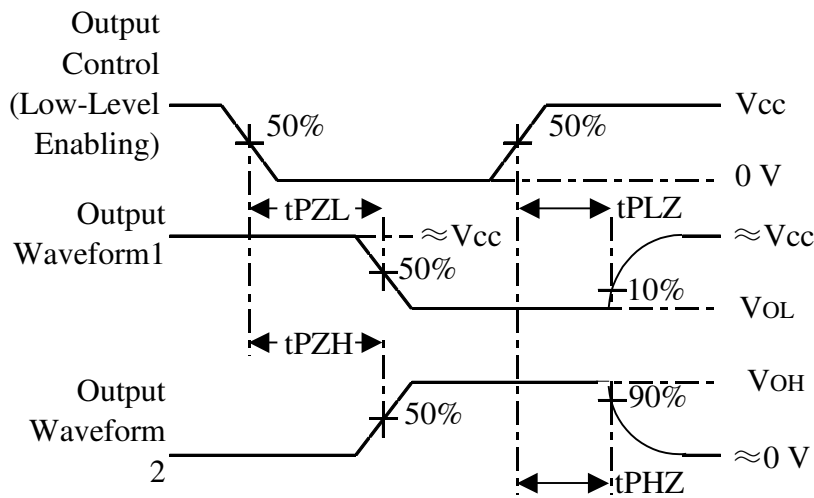
PARAMETER	RL	CL	S1	S2
ten	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
tdis	1 k Ω	50 pF	Open	Closed
			Closed	Open
tpd or tt	-	50 pF or 150 pF	Open	Open

AC SWITCHING WAVEFORM AND AC TEST CIRCUIT

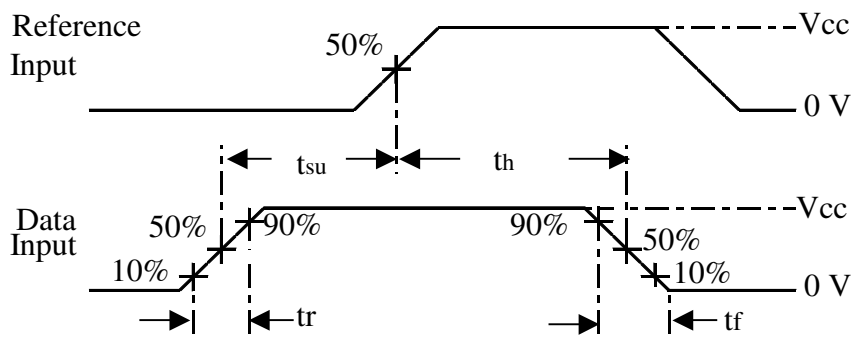
Voltage Waveforms 1. Propagation Delay and Output Transition Times



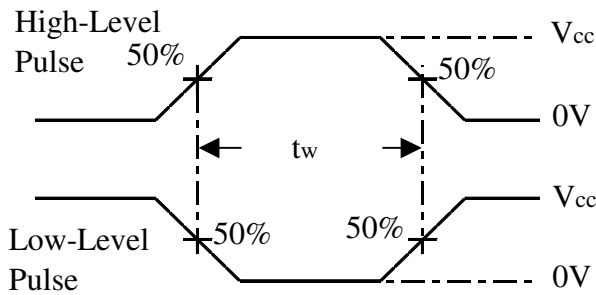
Voltage waveforms 2. Enable And Disable Times For 3-State Outputs



Voltage waveforms 3. Setup And Hold and Input Rise And Fall Times



Voltage waveforms 4. Pulse Durations

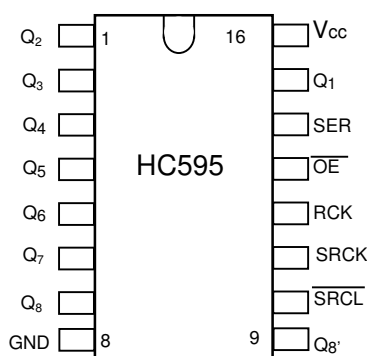


**Note:**

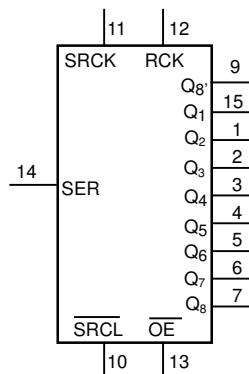
5. CL includes probe and test-fixture capacitance.
6. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $ZO = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
7. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
8. The outputs are measured one at a time, with one input transition per measurement.
9.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
10.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
11.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**PIN DESCRIPTION**

PIN NO.	SYMBOL	DESCRIPTION
15, 1, 2, 3, 4, 5, 6, 7	Q1 – Q8	Parallel data outputs
9	Q8'	Serial data output
10	SRCL	Shift register reset input (active low)
11, 12	SRCK, RCK	Shift and storage register clock inputs (triggered at positive edge)
13	OE	Output enable input (active low)
14	SER	Serial data input
8	GND	Ground (0V)
16	VCC	Positive power supply

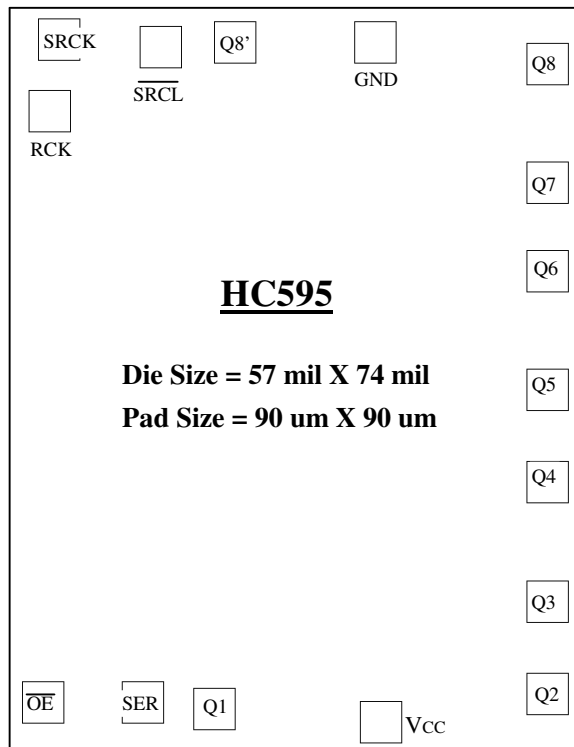


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

$\overline{OE}$ (-615.1, -748.2)	Q6 (479.8, 185.0)
SER (-398.1, -748.2)	Q7 (479.8, 379.6)
Q1 (-243.3, -762.4)	Q8 (479.8, 635.4)
VCC (118.3, -789.2)	GND (105.8, 683.3)
Q2 (479.8, -714.6)	Q8' (-199.4, 683.3)
Q3 (479.8, -520.6)	$\overline{SRCL}$ (-359.7, 673.2)
Q4 (479.8, -264.8)	SRCK (-581.0, 689.2)
Q5 (479.8, -70.2)	RCK (-600.9, 534.4)

**Note:** Substrate should be connected to Vcc or left it open.